Amendments to the Specification:

Replace the paragraph beginning on page 8, line 22 with the following amended paragraph:

With brief reference to FIGS. 1 and 2, if a request is made for the color attribute to be applied to pixel P0, the information from texture tile 14, namely texels T2, T4, T6 and T7 would be requested by fetch block 302 with such corresponding pixel information being maintained in texture caches 202-208 in corresponding order. In other words, the texture information for pixel P0 will be transferred to first texture cache 202; the texture information for pixel P1 will be transferred to second texture cache 204; the texture information for pixel P2 will be transferred to third texture cache 206 and the texture information for pixel P3 will be transferred to fourth texture cache 208. After the texture data has been transferred to the plurality of texture caches comprising the L1 cache, the requested information regarding, in this example, pixel P2 is then transferred from texture cache 206 to fetch block [[306]]302.

Replace the paragraph beginning on page 9, line 10 with the following amended paragraph:

After the fetch block [[306]]302 requests the information relating to pixel P2, the information relating to pixels P0-P3 are transferred from the main memory 102 into the L2 cache 104, via line 103, for storage. Once received, the information relating to pixel tile 14 is then transmitted to the appropriate texture cache (i.e. texture cache [[202]]206) for transfer to the requesting fetch block 302. The requested information is then transferred to the graphics controller 140 on line 107 for application to the point of interest.